FEATURES

1.0 PTP MASTER CLOCK

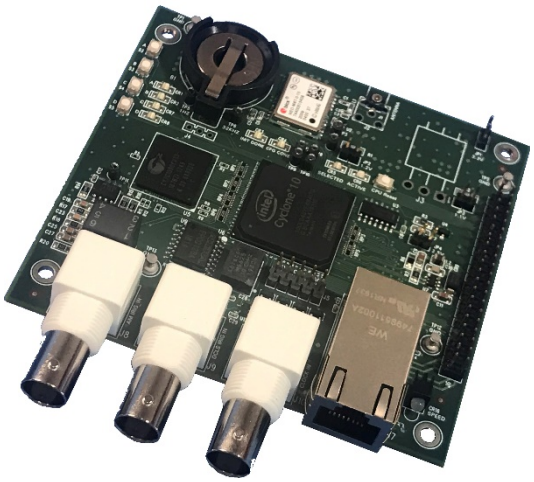
IEEE1588 V2 default profile; mode setting

2.0 12 CHANNEL GPS RECEIVER

Active GPS Patch Antenna Included

3.0 REFERENCE SYCHRONIZATION

External NTP Server or PTP Master Clock
Internal GPS (required for PTP master clock mode)
Any External IRIG B12x, format x=2-7External 1PPS clock reference (alternative for PTP master clock mode)



4.0 TIME OF DAY BATTERY BACKED UP CLOCK

5.0 10/100/1000 ETHERNET CONTROL, STATUS INTERFACE

Up to 10 concurrent client connections
Adjust all settings (command set), query time

6.0 WEBSERVER

Adjust all settings, display time and status

DESCRIPTION

When synchronized to the internal GPS, the Janus Time Engine Master Controller (JTEMC) may be set to perform as a local PTP Master Clock in accordance with IEEE standard 1588 V2 default profile. In Master Clock mode, the JTEMC can synchronize up to 10 devices on its network. It may also be used as a PTP Ordinary Clock. The JTEMC will then announce itself as a master clock periodically (settable). The sync packet rate is be programmable from 1/128 seconds to 128/sec in 15 steps. The system will be capable of synchronizing up to 10 PTPV2 slaves.

The JTEMC is may also perform as a PTP master clock when externally synchronized to a 1PPS, or IRIG B 00x (DCLS) time code signal. Using the embedded webserver, these references (GPS, 1PPS or IRIG B) may be set in a priority order to provide automated switchover if the currently selected time reference signal is lost.

Between reference switching or if all references are lost, the JTEMC disciplines its onboard OXCO to deliver an unlocked drift of less than 36 µS/Hr.

Synchronization to PTP as a slave or NTP as a client is achieved through the 10/100/1000 Ethernet port as is operation as PTP master clock. The interface supports both DHCP (default) and fixed IP address connections. All announce and slave-master communications will be accomplished via the GigE Ethernet port.

A Time Of Day (TOD) clock is provided that YYYY, MM, DD, HH, MM and SS values when powered down. The value of TOD is used to set the time master at power up. Time master accuracy is achieved after it has been synchronized to one of the available time reference sources.

The Janus Time Code Generate is an OEM PC board dimensionally compliant with PC104 specifications with a skyline dimension of 0.6 inches. Input power is +12 VDC at less than 5 watts.

There is an array of optional daughter I/O cards that provide time code signals for that may be used to synchronize other devices and provide phase locked and programmable frequency outputs. ITS also offers ODM design services to delivery custom I/O daughter cards the meet specific and unique needs.

ITS currently has designs and FPGA cores that provide:

- IRIG B time code generators programable as B127 (AM) or B007 (DCLS) synchronized to its time master
- Time master phase locked frequency generator programmable from 1Hz to 10 MHz in decade steps

- Time master phase locked frequency generator programmable from 1Hz to 1 KHz in 1 hertz steps

SPECIFICATIONS

PTP Master Clock

In order to be accepted by PTP slaves as a master clock the JTEMC must be synchronized to the internal GPS receiver or an external 1PPS, IRIG B00x timing source? As a PTP (IEEE 1588 V2) master clock and it can synchronize up to 10 PTP terminal (slave) devices on its local network.

GPS Synchronization

When Locked After Fix	Drift from last synchronized time when NOT locked
	After >20 min of GPS lock
±300 ns RMS @ 1 sec ±30 ns RMS @ 100 sec	< 36 µsec/hr. < 864 µsec/day

Active 3.5-5 VDC antenna SMA input. Compliant magnetic mount patch antenna with 5-meter cable is included.

PTP slave Synchronization

In PTP (IEEE 1588 V2) slave mode the system listens for a PTP master/boundary clock synchronization signals and will slave to the most local clock on the network to within 50±25 nanoseconds. This is a mutually exclusive selection with NTP. This mode is provided to support an array of optional I/O daughter cards that provides a variety of time code signals such as IRIG B12x, IRIG B00x, 1PPS, phase locked programmable frequency outputs and other timing signals.

NTP slave Synchronization

Client server relationship. Must have the address of a valid NTP server entered to synchronize. Time accuracy NTP 0±4 microseconds. Accuracy may vary outside this range dependent upon the stability of pathways, routers, and switches between the NTP server and the JTCG. This is a mutually exclusive selection with PTP.

1PPS Synchronization

A TTL 1PPS input may be applied which will synchronize the internal time master's one-second tick to the 1PPS input pulse. The actual year, day, HH, MM, SS is manually entered once between onesecond ticks.

IRIG B Input (2) Synchronization

IRIG B12x (IRIG Standard 200-04). Input level 1v p-p to 5 v p-p w/ mod ratio of 2:1 to 3:1. Formats (x) can be 0-7.
Note that IRIG B120-B123 do not encode the year. The year will appear as 2000 unless manually set.

IRIG B00x, DC Level Shift (DCLS) TTL input.
Note that IRIG B000-B003 do not encode the year. The year will appear as 2000 unless manually set.

GPS Position

Reports Latitude, Longitude and Altitude when locked to GPS. Outdoor position accuracy: 3-meter circular error probability (CEP) on query from the Ethernet port. Position data valid up to 50,000 meters (164K feet) altitude, 500 meter/sec (1,100 MPH) velocity with dynamics <=4g.

Package and Environment

Size Complies with PC104 dimensions, 3.55" x 3.775" x 0.600"

Weight	3.6 oz (100 g)	**Temp**	Op -30°C to +70°/ Non-Op -40°C to +85°	**Humidity**	85% non-condensing

Power Input

+12 VDC <5 watts

Webserver

IE11, Edge and Firefox compatible. Controls to set all parameters, display system time, synchronization source, lock status and the state of all settings.

Ordering Information

Part number 1412413, Product name: Janus Time Engine Master Controller

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